

Substitute for Form 1449 A &amp; B/PTO

Complete if Known

Application Number	09/693,976
Confirmation Number	8676
Filing Date	October 23, 2000
First Named Inventor	Albert E. CASAVANT
Art Unit	2121
Examiner Name	Aaron C. PEREZ DAPLE
Attorney Docket Number	A7675

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

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## U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
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## FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Translation <sup>6</sup>
		Country Code <sup>3</sup>	Number <sup>4</sup>	Kind Code <sup>5</sup> (if known)			

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## NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city, and/or country where published.	Translation <sup>6</sup>
		F. Balarin, et al., "An iterative approach to language containment," In Proceedings of the International Conference on Computer-Aided Verification, volume 697 of Lecture Notes in Computer Science, pages 29--40, 1993.	
		R. K. Brayton et al., "VIS: A system for verification and synthesis", In R. Alur and T. Henzinger, editors, Proceedings of the International Conference on Computer-Aided Verification, volume 1102, pages 428--432. Springer-Verlag, June 1996.	
		R. E. Bryant, "Graph-based algorithms for Boolean function manipulation", IEEE Transactions on Computers, C-35(8):677--691, Aug. 1986.	
		J. R. Burch, E. M. Clarke, D. E. Long, K. L. McMillan, and D. L. Dill, "Symbolic model checking for sequential circuit verification", IEEE Transactions on Computer-Aided Design, 13(4):401--424, Apr. 1994.	
		A. K. Chandra, et al., "Avpgen -- a test case generator for architecture verification", IEEE Transactions on VLSI Systems, 6(6), June 1995.	
		E. M. Clarke, et al., "Automatic verification of finite-state concurrent systems using temporal logic specifications", ACM Transactions on Programming Languages and Systems, 8(2):244--263, Apr. 1986.	
		E. M. Clarke, et al., "Counterexample-guided abstraction refinement", In Proceedings of the International Conference on Computer-Aided Verification, volume 1855 of Lecture Notes in Computer Science, pages 154--169, 2000.	
		F. Fallah, et al., "Functional vector generation for HDL models using linear programming and 3-Satisfiability", In Proceedings of the Design Automation Conference, pages 528--533, San Francisco, CA, June 1998.	
		M. Ganai, et al., "Augmenting simulation with symbolic algorithms", In Proceedings of the Design Automation Conference, June 1999.	
		D. Geist, et al., "Coverage-directed test generation using symbolic techniques", In Proceedings of the International Conference on Formal Methods in CAD, pages 143--158, Nov. 1996.	
		R. C. Ho, et al., "Architecture validation for processors", In Proceedings of the 22nd Annual International Symposium on Computer Architecture, June 1995.	
		Y. Hoskote, et al., "Coverage estimation for symbolic model checking", In Proceedings of the Design Automation Conference, pages 300--305, June 1999.	
		Y. Hoskote, et al., "Automatic extraction of the control flow machine and application to evaluating coverage of verification vectors", In Proceedings of the International Conference on Computer Design, pages 532--537, Oct. 1995.	
		C.-Y. Huang, et al., "Assertion checking by combined word-level ATPG and modular arithmetic constraint-solving techniques", In Proceedings of the Design Automation Conference, pages 118--123, 2000.	
		C. N. Ip, et al., "Using symbolic analysis to optimize explicit reachability analysis", In Proceedings of Workshop on High Level Design Validation and Test, 1999.	
		S. Katz, et al., "Have I Written Enough Properties? -- a method of comparison between specification and implementation", In Proceedings of Correct Hardware Design and Verification Methods (CHARME), volume 1703 of Lecture Notes in Computer Science, pages 280--297, Sep. 1999.	
		A. Kuchlmann, et al., "Probabilistic state space search", In Proceedings of the International Conference on Computer-Aided Design, 1999.	

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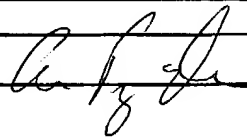
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		W. Lee, et al., "Tearing based abstraction for CTL model checking", In Proceedings of the International Conference on Computer-Aided Design, pages 76--81, San Jose, CA, Nov. 1996.	
		J. Lind-Nielsen, et al., "Stepwise CTL model checking of state/event systems", In Proceedings of the International Conference on Computer-Aided Verification, volume 1633 of Lecture Notes in Computer Science, pages 316--327. Springer-Verlag, 1999.	
		D. E. Long, Model Checking, Abstraction and Modular Verification, PhD thesis, School of Computer Science, Carnegie Mellon University, Pittsburgh, PA, July 1993.	
		A. Pardo, et al., "Automatic abstraction techniques for propositional $\mu$ -calculus model checking", In Proceedings of the International Conference on Computer Aided Verification, volume 1254 of Lecture Notes in Computer Science, pages 12--23, June 1997.	
		R. Summers, et al., "Improving witness search using orders on states", In Proceedings of the International Conference on Computer Design, pages 452--457, 1999.	
		Synopsys, Inc. VERA System Verifier, <a href="http://www.synopsys.com/products/vera/vera.html">http://www.synopsys.com/products/vera/vera.html</a>	
		TransEDA, Inc. Verification Navigator, <a href="http://www.transeda.com">http://www.transeda.com</a>	
		Verisity Design, Inc. Specman Elite, <a href="http://www.verisity.com/html/specmanelite.html">http://www.verisity.com/html/specmanelite.html</a>	
		K. Wakabayashi, "C-based Synthesis Experiences with a Behavior Synthesizer "Cyber" ", In Proceedings of the Design Automation and Test in Europe (DATE) Conference, pages 390--393, 1999.	
		C. Han Yang, et al., David L. Dill, "Validation with guided search of the state space", In Proceedings of the Design Automation Conference, June 1998.	
		J. Yuan, et al., "On combining formal and informal verification", In Proceedings of the International Conference on Computer-Aided Verification, volume 1254 of Lecture Notes in Computer Science, pages 376--387, June 1997.	

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